Superconducting TES Array Electronics Block Diagrams

The array block diagrams in this document consist of a variety of setups for operating Nx32 detectors.

It is assumed that the final arrays require 32 pairs for addressing (derived from a cryogenic address driver).
This requires a single 65-pin nanonics connector with no termination anywhere unless it is added onto the detector package itself to better match the impedance of the twisted pairs.

It is further assumed that each column requires 1st FB, Detector Bias, and 2nd FB to be wired to the package.
The package must have each column's 2nd Out wired to the SA housing.
The SA housing will require a 3rd FB and 3rd Out to connect to the RT electronics.

I have made the choice to wire the 2nd Bias to the SA housing, which has a few benefits:
- requires fewer wires to the cold stage
- doesn't put a load resistor on the cold stage
- permits the flex-to-nanonics boards to be in units of 3 flex lines for both the SA and the Detector wiring.

For the test package (2x32), it is assumed that we will have two different packages with the same connector layout.
- One package will be set up exactly as a 2x32 mux, with an extra detector bias per column.
- One package will be set up to run 4 devices straight to the SA, and with six 4-wire test points.

Additionally, the GBT arrays will be set up the same way as the Nx32, but with most address wires disabled.

Current Calculations:

Detector bias will drop ~1µV across a ~1mΩ shunt, so if we use a 1kΩ load resistor, we must produce 1V @300K.
Dissipation at 2K is about 1mW per column.
1st FB is ~1µA and gets a 50Ω/50Ω termination, so we produce only ~200µV and dissipate ~nW at 2K.

2nd Bias requires ~100µA thru 1Ω with 0.1Ω shunt so ~1mA total.
Assume 50Ω of flex, and we put a 50Ω/50Ω termination @2K, so 200mV range @300K. 2K dissipation 400µW/col.
2nd FB requires ~10µA or so, so we terminate with 50Ω/1kΩ at 2K and require 20mV @300K. 2K dissipation 4µW/col.

3rd Bias requires ~100µA and has no termination. Dissipation is ~1µW at 2K. Need 10mV @300K.
3rd FB requires ~10µA, so we put a 50Ω/1kΩ termination to yield 20mV @300K, dissipating 4µW/col at 2K.

The total dissipation at 2K is very roughly 2mW/column, a not insignificant amount.

Notes on components:
The singly-hatched cables are Nb/Ti wires with Cu/Ni cladding, in twisted pairs of 0.003" conductors woven by TekData.
The doubly-hatched cables are wires mated to the Nanonics connectors at the factory..
I have chosen Nanonics connectors to keep everything small. The wire count is kept lowest if we use:
65 pin connectors for the 64 address wires
51 pin connectors for the 48 wires to SA and "Inputs"
25 pin connectors for the 16 wires to the "Outputs"
The connection between the SA housing and the Flex lines will be made by buying Nanonics connectors with wires.
These wires will be soldered to the Flex Termination Board.

In order to minimize the total number of connectors, each circuit board is supplied with one hard-mounted connector end and one TekData cable soldered & strain relieved end.

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Parts List:

Tower Cards:

10 Power cards (SAFIRE, SPIFI, GBT, Princeton, Purple & spares)
10 Address Interface cards (as above)
13 DAC cards (standard)
15 Modified DAC cards (2 passthru channels)
15 Passthru cards (standard)
20 Passthru cards (partially isolated)
15 PreAmp cards (standard)
15 PreAmp cards (half or more working; duplicates above)

Cold Cards:

14 SA Mount cards (SAFIRE, SPIFI, GBT, Princeton, Purple & spares)
10 Address Driver cards (as above)

Crate Cards:

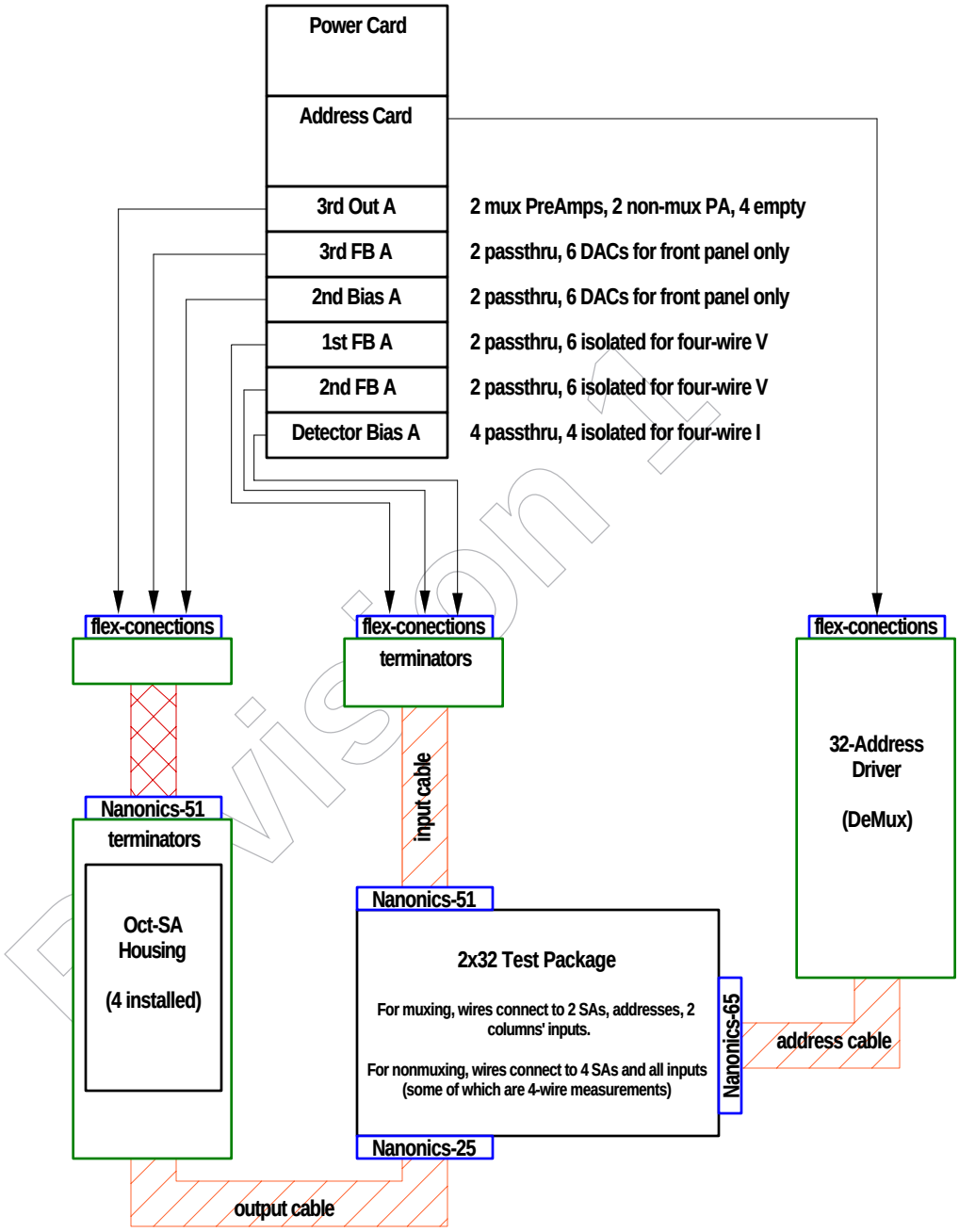
70 Column Controller cards (SAFIRE, SPIFI, GBT, Princeton, Purple & spares)
10 Clock cards (as above)

Computer Cards:

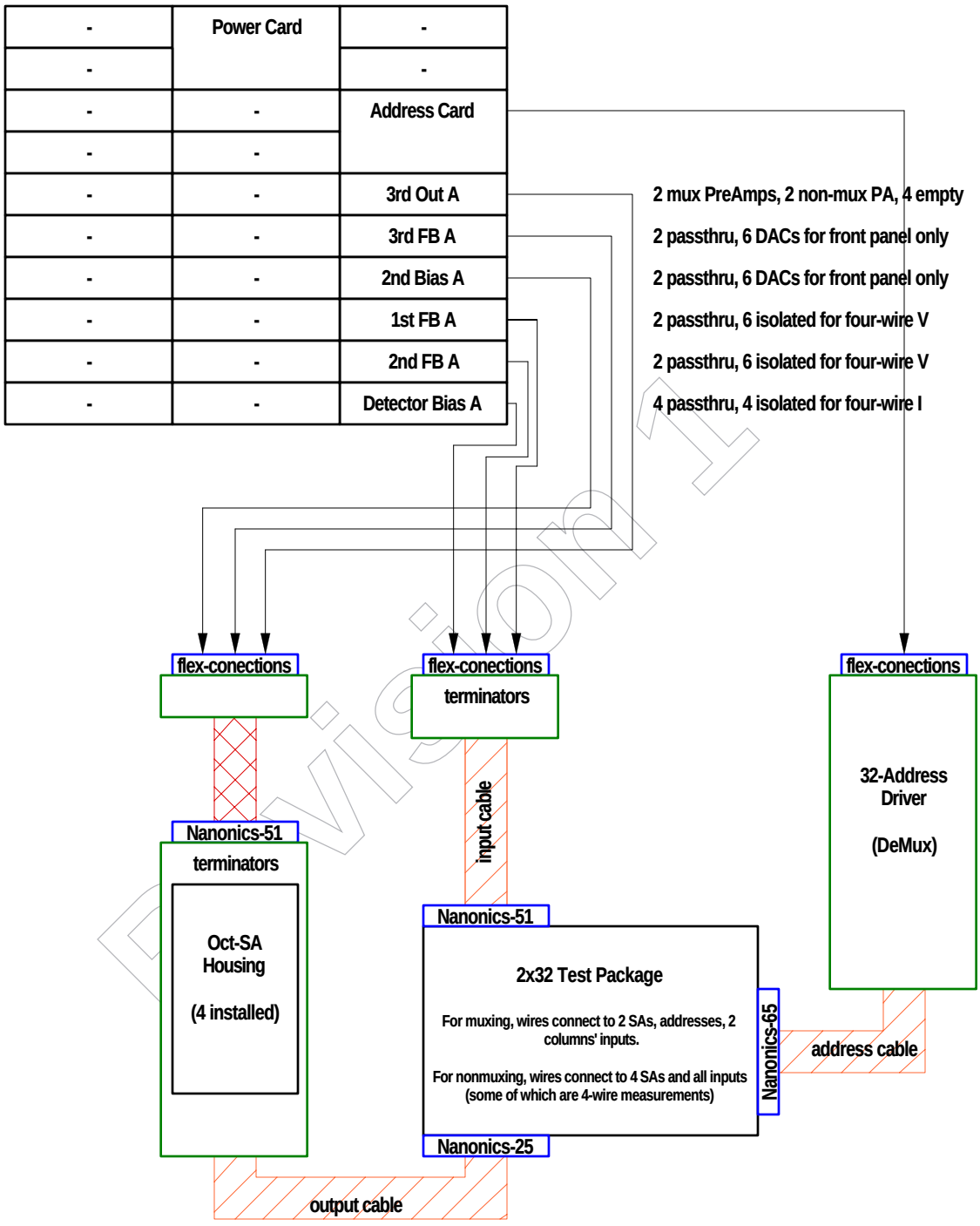
10 PCI cards (SAFIRE, SPIFI, GBT, Princeton, Purple & spares)

Note on spares: I have assumed for all cards that GSFC gets 2 each while Penn, Princeton, and Cornell get 1 each. This may be more than necessary if we're willing to ship cards around to cover failures.

GSFC Research (Purple Dewar): 2x32 Test Array Electronics Block Diagram

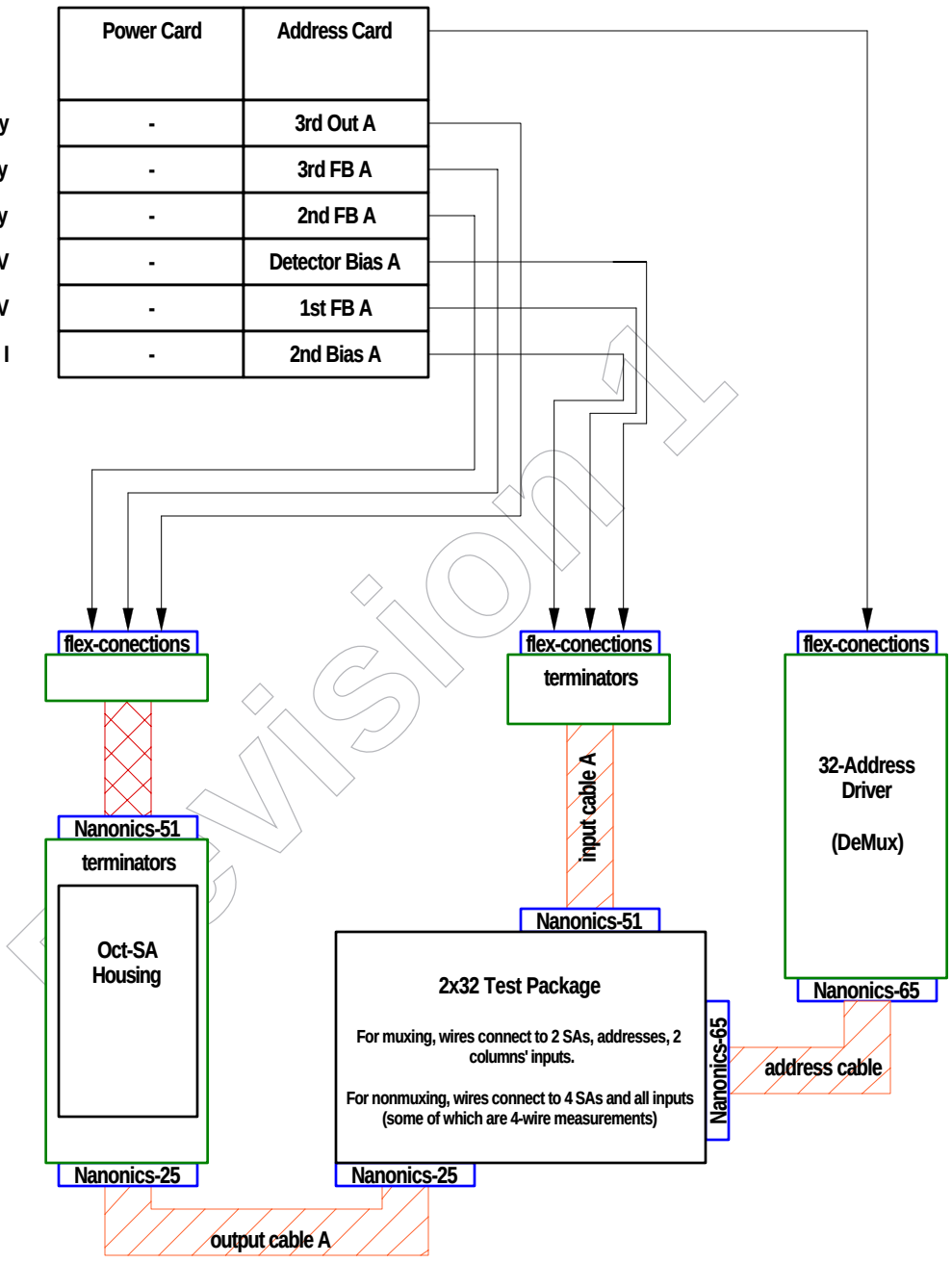


SAFIRE: 2x32 Test Array Electronics Block Diagram

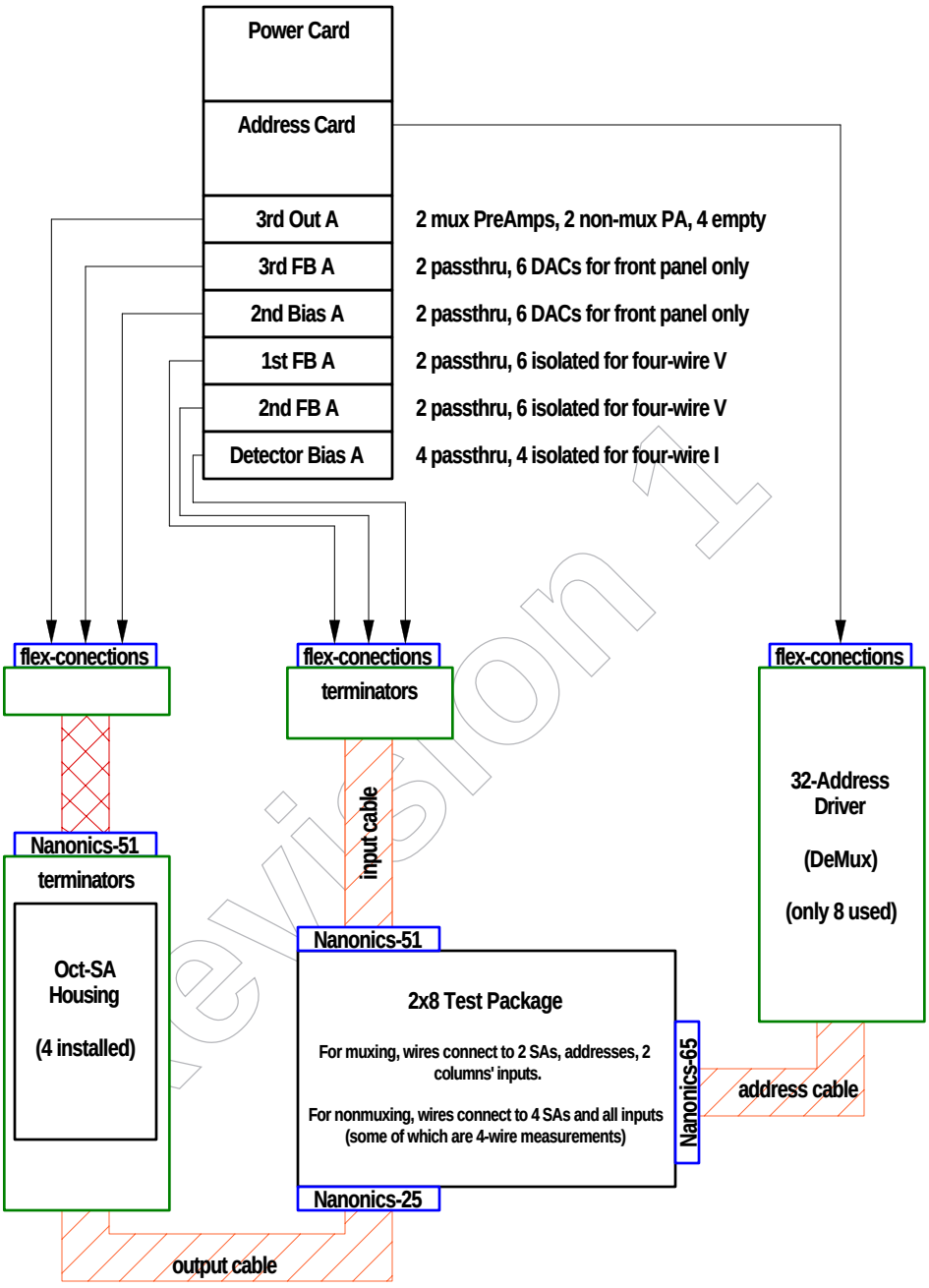


SPIFI: 2x32 Test Array Electronics Block Diagram

	Power Card	Address Card
2 mux PreAmps, 2 non-mux PA, 4 empty	-	3rd Out A
2 passthru, 6 DACs for front panel only	-	3rd FB A
2 passthru, 6 DACs for front panel only	-	2nd FB A
2 passthru, 6 isolated for four-wire V	-	Detector Bias A
2 passthru, 6 isolated for four-wire V	-	1st FB A
4 passthru, 4 isolated for four-wire I	-	2nd Bias A

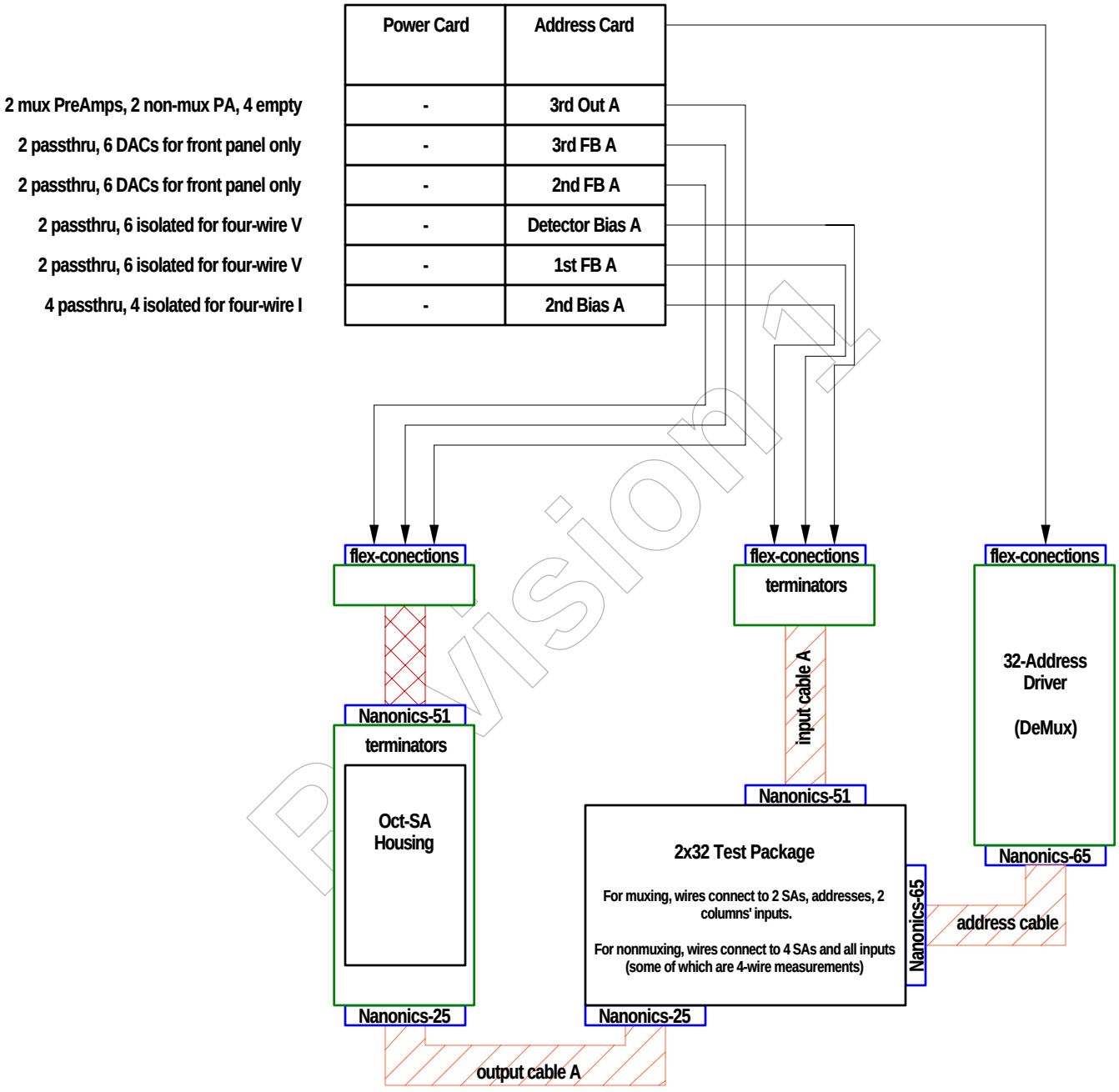


Penn/GBT: 2x8 Test Array Electronics Block Diagram

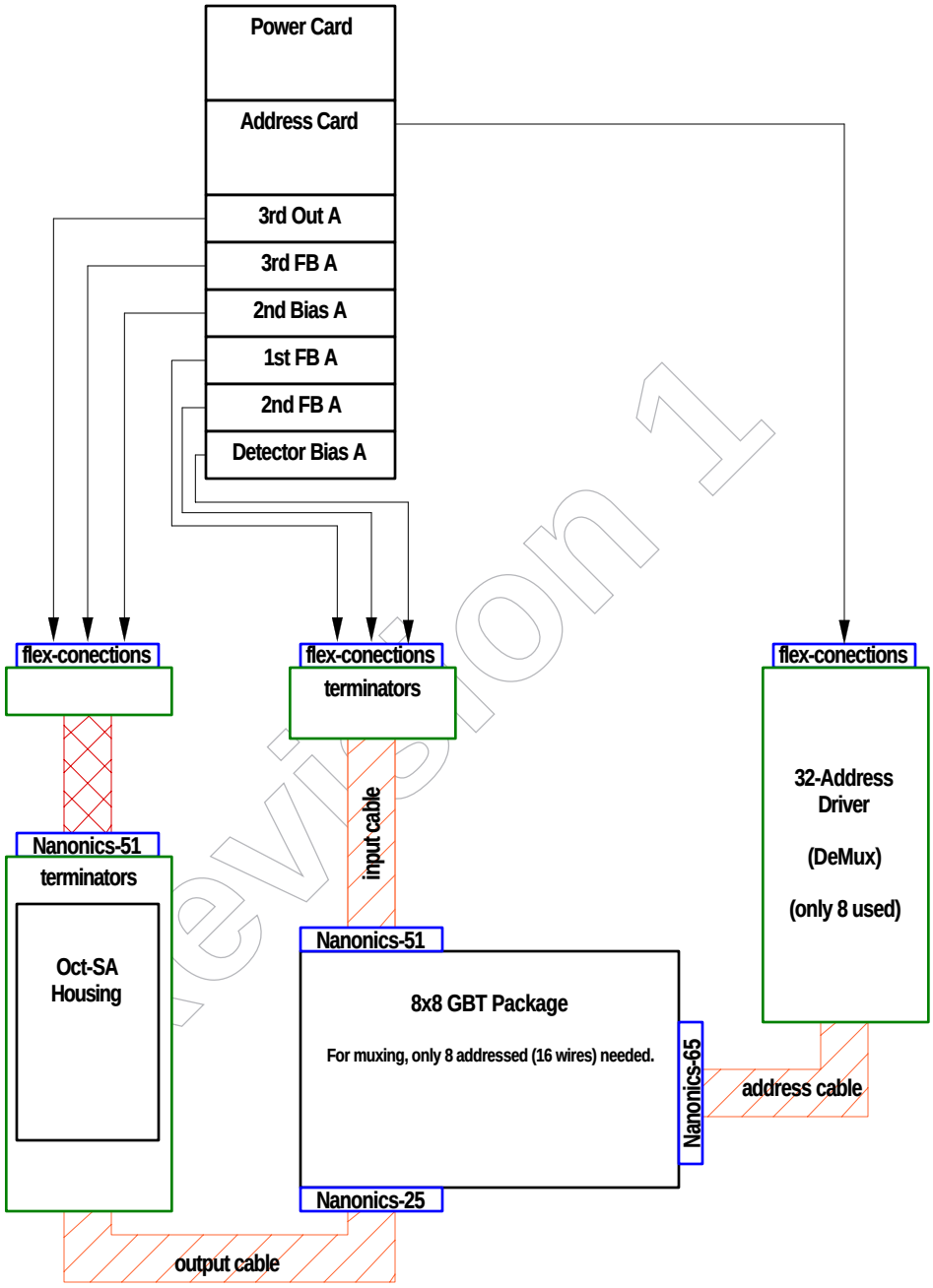


Princeton: 2x32 Test Array Electronics Block Diagram

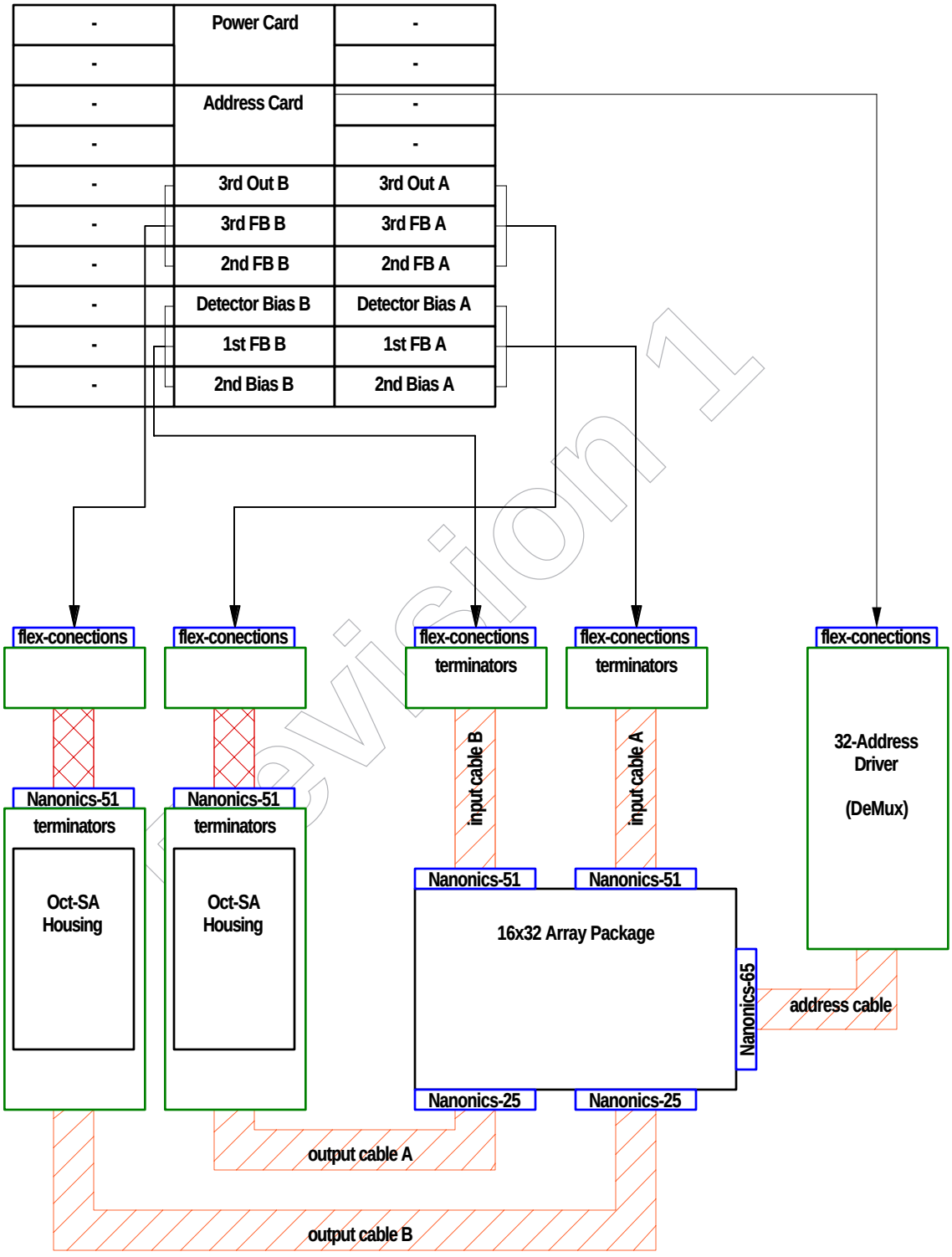
(expandable to 16x32 with no changes; subject to Princeton approval)



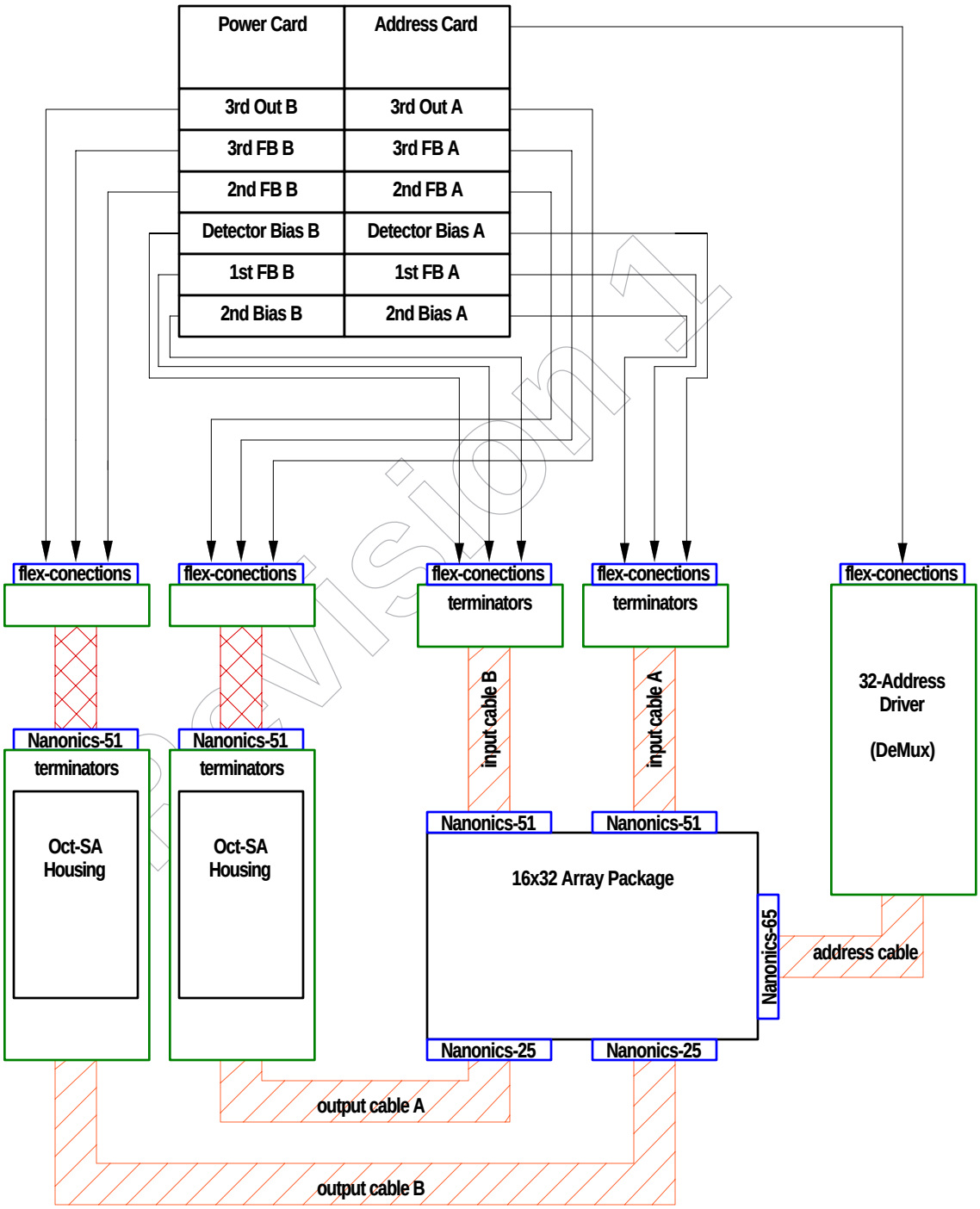
Penn/GBT: 8x8 Array Electronics Block Diagram



SAFIRE: 16x32 Array Electronics Block Diagram



SPIFI: 16x32 Array Electronics Block Diagram



SAFIRE: 32x32 Array Electronics Block Diagram

-	Power Card	-
3rd Out D		Detector Bias D
3rd FB D	Address Card	1st FB D
2nd FB D		2nd Bias D
3rd Out C	3rd Out B	3rd Out A
3rd FB C	3rd FB B	3rd FB A
2nd FB C	2nd FB B	2nd FB A
Detector Bias C	Detector Bias B	Detector Bias A
1st FB C	1st FB B	1st FB A
2nd Bias C	2nd Bias B	2nd Bias A

flex-conections
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terminators
flex-conections
terminators
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terminators
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terminators
flex-conections
32-Address Driver
(DeMux)
address cable
input cable B
input cable A
input cable C
input cable D
Nanonics-51
terminators
Oct-SA Housing
Nanonics-51
terminators
Oct-SA Housing
Nanonics-51
terminators
Oct-SA Housing
Nanonics-51
terminators
Oct-SA Housing
Nanonics-51
Nanonics-51
Nanonics-51
Nanonics-51
32x32 Array Package
Nanonics-65
Nanonics-25
Nanonics-25
Nanonics-25
Nanonics-25
output cable A
output cable B
output cable C
output cable D